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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,417	03/08/2001	Hidekazu Watanabe	80398P348	5418
8791	7590	09/18/2003		
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD, SEVENTH FLOOR LOS ANGELES, CA 90025				EXAMINER LEFKOWITZ, SUMATI
			ART UNIT 2189	PAPER NUMBER

DATE MAILED: 09/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicant No.	Applicant(s)
	09/802,417	WATANABE, HIDEKAZU
	Examiner	Art Unit
	Sumati Lefkowitz	2189

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 13 August 2001.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-30 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 08 March 2001 is/are: a) accepted or b) objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-30 are pending.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.
3. The abstract of the disclosure is objected to because
 - it fails to mention that the bus controller has two modes of operations, one in which it allows the buses to operate independently of one another and another mode in which it allows the buses to operate in conjunction with one anotherCorrection is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
5. Claims 1-7, 9-17, 19-27, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jahnke et al., US 2002/0052999 A1 (hereinafter Jahnke) in view of Gehman et al., 6,260,093 (hereinafter Gehman).

As to claims 1-7, 9-17, 19-27, 29, and 30, Jahnke discloses an apparatus (note Figure 3, elements 314, 315, 316) comprising first (note Figure 3, element 314 and circuitry internal to bridge 315 for interfacing with AHB bus) and second (note Figure 3, element 316 and circuitry internal to bridge 315 for interfacing with HTB bus) bus interface circuits to interface to first (note Figure 3, AHB bus 300) and second (note Figure 3, HTB bus 330) buses, respectively, the first bus being accessible to a first processor (note Figure 3, CPU 301), a processor interface circuit (note Figure 3, element 316) to interface to a second master (note Figure 3, element 333), and an arbitration logic circuit (note Figure 3, elements 314 and 316) coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first processor and second master, wherein the second master is coupled to the first and second buses (note Figure 3, wherein the second master 333 is coupled to the second bus 330 and the first bus 300 through bridge 315), wherein the processor interface circuit comprises a command decoder to decode an access command from the second processor requesting access to one of the first and second buses (note [0025], wherein the fact that HTB peripheral requests and is granted control of HTB bus implies that a command decoder is present to decode the access request from the peripheral), wherein the arbitration circuit disables the first bus interface circuit when the second processor requests access to the second bus or that the arbitration circuit enables the first and second bus interface circuits when access request to the second bus from the first processor is granted (i.e., inherent in the fact that the bridges allow for independent, concurrent access or isolation of the buses from each other, which would imply that the interfaces, including inherent drivers and receivers, would be disabled to prevent any collisions on the bus, i.e., to insure that only one master has access to each bus at any given time and that

the bridges also allow for transactions to cross the bridge, which would imply that the interfaces, including inherent drivers and receivers, would have to be enabled to allow transactions to cross the bridge from one bus to the other), wherein the arbitration logic circuit resolves access requests from the first processor and second master such that the first processor accesses the first bus while the second master accesses the second bus ([0019], wherein the bridge providing isolation between the buses reads on the first processor accessing the first bus while the second master accesses the second bus), wherein the first processor is one of a microprocessor, a micro-controller, and a digital signal processor (note Figure 3, CPU 301), wherein the first and second buses are of different types (note AHB bus and HTB bus), further discloses a method comprising interfacing to first (AHB bus) and second buses (HTB bus) by first (note Figure 3, element 314 and circuitry internal to bridge 315 for interfacing with AHB bus) and second (note Figure 3, element 316 and circuitry internal to bridge 315 for interfacing with HTB bus) interface circuits, respectively, the first bus being accessible to a first processor (note Figure 3, CPU 301), interfacing to a second master (note Figure 3, HTB peripheral 333), and arbitrating access requests from the first processor and second master, wherein the second master is coupled to the first and second buses, further discloses a system comprising first (i.e., APB bus) and second (i.e., HTB bus) buses, first processor (note Figure 3, CPU 301) and second master (note Figure 3 HTB peripheral 333), the first processor being coupled to the first bus, a bus controller (note Figure 3, elements 314, 315, and 316) coupled to the first and second buses to control bus access from the first processor and second master, the bus controller comprising first (note Figure 3, element 314 and circuitry internal to bridge 315 for interfacing with AHB bus) and second (note Figure 3, element 316 and circuitry internal to bridge 315 for interfacing with HTB bus) bus

interface circuits to interface to the first and second buses, respectively, a processor interface circuit (note Figure 3, element 316) to interface to the second master, and an arbitration logic circuit (note Figure 3, elements 314 and 316) coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first processor and second master (note Figure 3, [0006-0007, 0017-0028]).

Jahnke fails to disclose that the second master is a processor or that the buses are the same buses.

Gehman discloses that the second master is a processor and that the buses are the same buses (note column 3, lines 8-59).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of a processor as the second master so as to allow for the use of intelligent peripherals in the system of Jahnke, as Gehman teaches in column 3, lines 33-36, thereby increasing the functionality of the system of Jahnke.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the buses be the same buses, as Gehman teaches, in the system of Jahnke so as to allow for the addition of more devices, even when existing buses have been loaded to their maximum.

6. Claims 1-7, 11-17, and 21-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crews et al., 5,619,661 (hereinafter Crews) in view of Gehman et al., 6,260,093 (hereinafter Gehman).

As to claims 1-7, 11-17, and 21-27, Crews discloses an apparatus (note Figure 1, bridge

chip 30) comprising first (note Figure 1, elements 32, 42, 40) and second (note Figure 1, elements 36, 38, 34) bus interface circuits to interface to first (note Figure 1, primary bus 10) and second (note Figure 1, secondary bus 20) buses, respectively, the first bus being accessible to a first processor (note column 1, lines 9-12), a processor interface circuit (note Figure 1, elements 32, 42, 40) to interface to a second master (note Figure 1, element 18), and an arbitration logic circuit (note Figure 1, elements 32 and 34) coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first processor and second master, wherein the arbitration circuit disables the first bus interface circuit when the second processor requests access to the second bus or that the arbitration circuit enables the first and second bus interface circuits when access request to the second bus from the first processor is granted (i.e., inherent in the fact that the bridges allow for independent, concurrent access, which would imply that the interfaces, including inherent drivers and receivers, would be disabled to prevent any collisions on the bus, i.e., to insure that only one master has access to each bus at any given time and that the bridges also allow for transactions to cross the bridge, which would imply that the interfaces, including inherent drivers and receivers, would have to be enabled to allow transactions to cross the bridge from one bus to the other), wherein the second master is coupled to the first and second buses (note Figure 1, wherein the second master 18 is coupled to the second bus 20 and to the first bus 10 through bridge 30), wherein the processor interface circuit comprises a command decoder to decode an access command from the second processor requesting access to one of the first and second buses (note column 5, lines 22-55, wherein the fact that secondary to primary bus transfer requests are granted implies that a command decoder is present to decode the access request from the master on the secondary bus), wherein the

arbitration logic circuit resolves access requests from the first processor and second master such that the first processor accesses the first bus while the second master accesses the second bus (note column 3, lines 58 – column 4, line 52), wherein the first processor is one of a microprocessor, a micro-controller, and a digital signal processor (note column 1, lines 9-12), further discloses a method comprising interfacing to first (i.e., primary bus 10) and second (i.e., secondary bus 20) bus by first (note Figure 1, elements 32, 42, 40) and second (note Figure 1, elements 36, 38, 34) interface circuits, respectively, the first bus being accessible to a first processor (note column 1, lines 9-12), interfacing to a second master (note Figure 1, master 18), and arbitrating access requests from the first processor and second master, wherein the second master is coupled to the first and second buses, further discloses a system comprising first (i.e., primary bus 10) and second (i.e., secondary bus 20) buses, first processor (note column 1, lines 9-12) and second master (note column 1, master 18), the first processor being coupled to the first bus, a bus controller (note Figure 1, bridge 30) coupled to the first and second buses to control bus access from the first processor and second master, the bus controller comprising first (note Figure 1, elements 32, 42, 40) and second (note Figure 1, elements 36, 38, 34) bus interface circuits to interface to the first and second buses, respectively, a processor interface circuit (note Figure 1, elements 32, 42, 40) to interface to the second master, and an arbitration logic circuit (note Figure 1, elements 32 and 34) coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first processor and second master (note Figure 1 and column 3, line 58 – column 5, line 55).

Crews fails to disclose that the second master is a processor.

Gehman discloses that the second master is a processor (note column 3, lines 8-59).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of a processor as the second master so as to allow for the use of intelligent peripherals in the system of Crews, as Gehman teaches in column 3, lines 33-36, thereby increasing the functionality of the system of Crews.

7. Claims 8, 18, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jahnke et al., US 2002/0052999 A1 (hereinafter Jahnke) in view of Gehman et al., 6,260,093 (hereinafter Gehman), as applied to claims 1-7, 9-17, 19-27, 29, and 30 above, and further in view of Mergard et al., 5,941,968 (hereinafter Mergard).

As to claims 8, 18, and 28, fails to disclose that the second processor is a DMAC.

Mergard discloses that the second processor is a DMAC (note Figures 1A, 1B, DMA Controller 122).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of a DMAC as the second processor so as to relieve the CPU of the burden of performing memory transfers.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the prior art teaches or suggests using a bridge to independently transfer data on each bus connected by the bridge and to transfer data from one bus to the other across the bridge and/or arbitration for a common bus.

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6,070,205	Kato et al.
5,764,933	Richardson et al.
5,675,751	Baker et al.

5,790,870	Hausauer et al.
5,761,454	Adusumilli et al.
5,546,546	Bell et al.

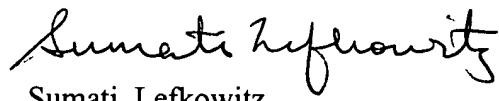
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sumati Lefkowitz whose telephone number is 703-308-7790. The examiner can normally be reached on Monday-Friday from 6:00-2:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached at 703-305-4815.

The fax phone numbers for the organization where this application or proceeding is assigned are:

703-746-7238	for After-Final communications
703-872-9306	for Official communications
703-746-5661	for Non-Official/Draft communications

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.


Sumati Lefkowitz
Primary Examiner
Art Unit 2189

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September 12, 2003